Product Introduction

G32A1445

Arm® Cortex® -M4F core-based 32-bit MCU

December, 2023

1 Product Characteristics

Core

- 32-bit Arm® Cortex® -M4F core with FPU
- Up to 112MHz working frequency

Memory and interface

- Flash: Up to 512KB
- SRAM:64KB
- 64KB Data Flash with ECC
- 4KB FlexRAM for use as SRAM or EEPROM

Clock

- HSE: 4~40MHz external crystal/ceramic oscillator supported
- HSI: 48MHz RC oscillator calibrated by factory
- LSI: 8MHz RC oscillator supported
- LPO: 128 kHz low-power oscillator
- SYSPLL: 112MHz main phase-locked loop

Power supply and power supply management

- VDD range: 2.7V~5.5V
- VDDA range: 2.7V~5.5V
- Power-on/low-power reset (POR/LVR) supported
- Low-voltage detector (LVD) supported

DMA

- 16 channels

Debugging Interface

- SWJ-DP
- DWT
- ITM
- TPIU
- FPB

I/O

- Up to 89 I/Os
- All I/O can be mapped to external interrupt vector

Communication peripherals

- 1×LPI2C interface
- 3×LPUART
- 3×LPSPI
- 3×FlexCAN (all support CAN FD)

Analog peripherals

- 2×12-bit ADC
- 1×comparator with internal 8-bit DAC
- 2×programmable delay module PDUs with flexible trigger system

Timer

- 4×independent 16-bit FTMR modules, offering up to 32 standard channels
- 1×16-bit LPTMR with flexible wake-up control
- 1×32-bit LPITMR with 4-channel
- 1 × RTC, support calendar function, support alarm and regular wake-up from stop/standby mode

Safety and Security

- Cryptographic Services Engine (CSEc) implements a complete set of encryption capabilities described in the SHE (Secure Hardware Extension) functional specification
- 128-bit unique device ID
- CRC computing unit
- 1×internal watchdog(WDT)
- 1×external watchdog monitor(EWDT)
- System Memory Protection Unit(MPU)
- ECC on FLASH and SRAM

Chip package

- LQFP64
- LQFP100

Contents

2 Product Information

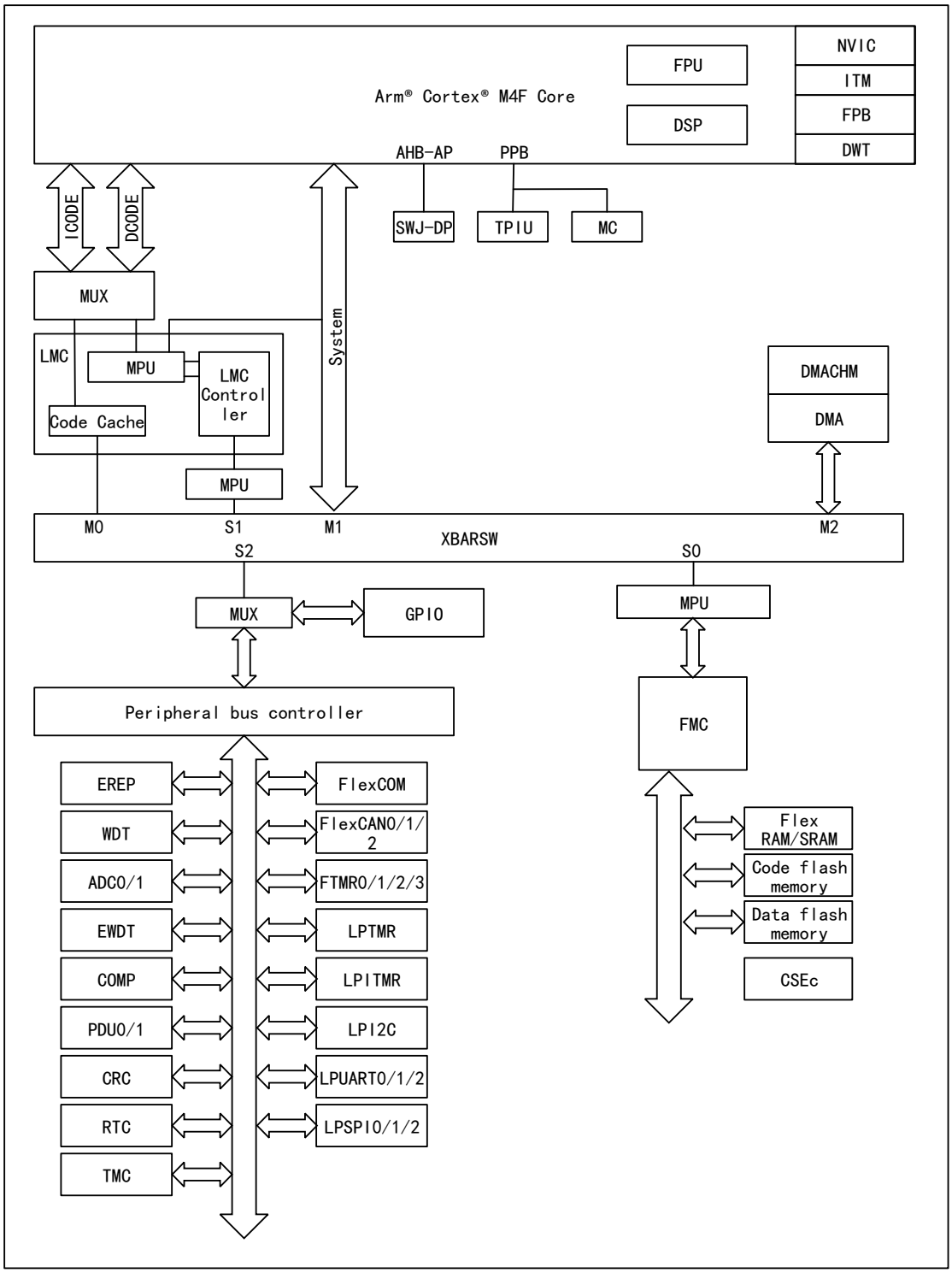
See the following table for G32A1445 product functions and peripheral configuration.

Table 1 Functions and Peripherals of G32A1445 Series Chips

Product		G32A1445							
Model		UAT0MLH	HAT0MLH	UAT0VLH	HAT0VLH	UAT0MLL	HAT0MLL	UAT0VLL	HAT0VLL
Package		LQFP64				LQFP100			
Core		Arm® 32-bit Cortex®-M4F							
Maximum operating frequency (MHz)		112	80	112	80	112	80	112	80
Working voltage		2.7-5.5V							
Flash (KB)		512							
SRAM (KB)		64							
GPIOs		58				89			
Communication interface	LPUART	3							
	LPSPI	3							
	LPI2C	1							
	CAN	3							
Timer	16-bit FTMR	4							
	16-bit LPTMR	1							
	32-bit LPITMR	1							
	Watchdog	2							
Real-time clock		1							
12-bit ADC	Unit	2							
	External channel	16+13				16+16			
8-bit DAC	Unit	1							
Analog comparator		1							
PDU		2							
Operating temperature		Ambient temperature: -40°C to 125°C Junction temperature: -40℃ to 135℃		Ambient temperature: -40°C to 105°C Junction temperature: -40℃ to 125℃		Ambient temperature: -40°C to 125°C Junction temperature: -40℃ to 135℃		Ambient temperature: -40°C to 105°C Junction temperature: -40℃ to 125℃	

3 System Block Diagram

Figure 1 System Block Diagram



4 Pin Configuration and Functions

Figure 2 64-Pin LQFP Top View

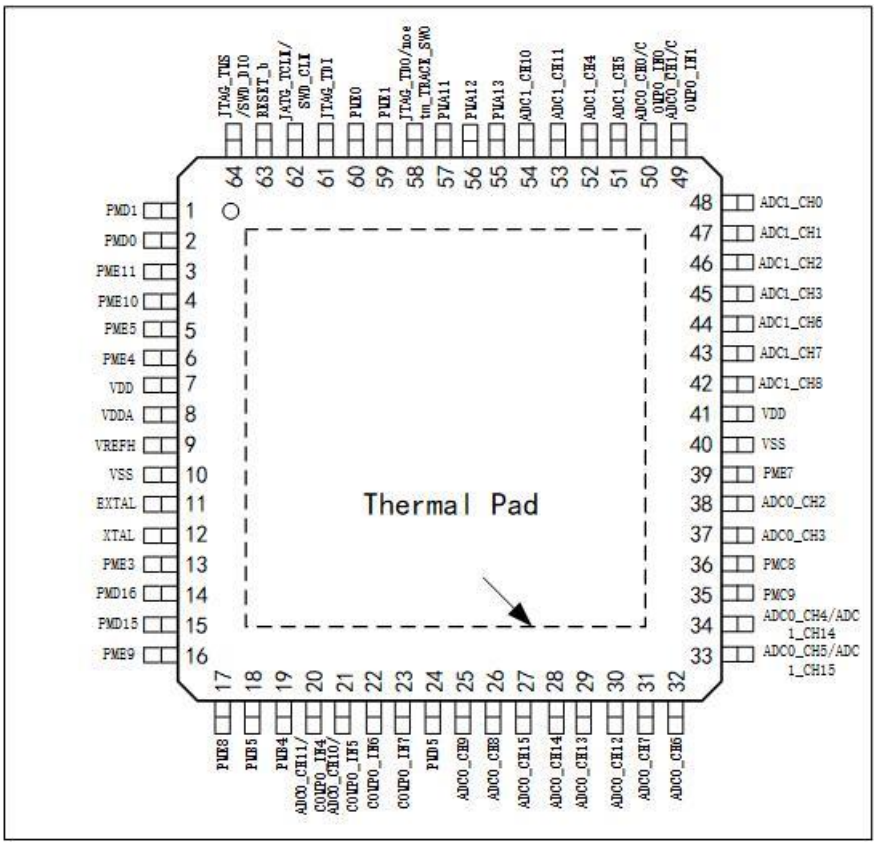


Table 2 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA0	50	I/O	Default:ADC0_CH0/COMP0_IN0(ADC0 channel 0/COMP0 input channel 0)
PMA1	49	I/O	Default:ADC0_CH1/COMP0_IN1(ADC0 channel 1/COMP0 input channel 1)
PMA2	48	I/O	Default:ADC1_CH0(ADC1 channel 0)
PMA3	47	I/O	Default:ADC1_CH1(ADC1 channel 1)
PMA4	64	I/O	JTAG_TMS/SWD_DIO
PMA5	63	I/O	RESET_b
PMA6	38	I/O	Default:ADC0_CH2(ADC0 channel 2)
PMA7	37	I/O	Default:ADC0_CH3(ADC0 channel 3)
PMA10	58	I/O	JTAG_TDO/noetm_TRACE_SWO
PMA11	57	I/O	GPIO

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA12	56	I/O	GPIO
PMA13	55	I/O	GPIO
PMB0	34	I/O	Default:ADC0_CH4/ADC1_CH14(ADC0 channel 4/ ADC1 channel 14)
PMB1	33	I/O	Default:ADC0_CH5/ADC1_CH15(ADC0 channel 5/ ADC1 channel 15)
PMB2	32	I/O	Default:ADC0_CH6(ADC0 channel 6)
PMB3	31	I/O	Default:ADC0_CH7(ADC0 channel 7)
PMB4	19	I/O	GPIO
PMB5	18	I/O	GPIO
PMB6	12	I/O	XTAL
PMB7	11	I/O	EXTAL
PMB12	43	I/O	Default:ADC1_CH7(ADC1 channel 7)
PMB13	42	I/O	Default:ADC1_CH8/ADC0_CH8(ADC1 channel 8/ADC0 channel 8)
PMC0	26	I/O	Default:ADC0_CH8(ADC0 channel 8)
PMC1	25	I/O	Default:ADC0_CH9(ADC0 channel 9)
PMC2	21	I/O	Default:ADC0_CH10/COMP0_IN5(ADC0 channel 10/COMP0 channel 5)
PMC3	20	I/O	Default:ADC0_CH11/COMP0_IN4(ADC0 channel 11/COMP0 channel 4)
PMC4	62	I/O	JTAG_TCLK/SWD_CLK
PMC5	61	I/O	JTAG_TDI
PMC6	52	I/O	Default:ADC1_CH4(ADC1 channel 4)
PMC7	51	I/O	Default:ADC1_CH5(ADC1 channel 5)
PMC8	36	I/O	GPIO
PMC9	35	I/O	GPIO
PMC14	30	I/O	Default:ADC0_CH12(ADC0 channel 12)
PMC15	29	I/O	Default:ADC0_CH13(ADC0 channel 13)
PMC16	28	I/O	Default:ADC0_CH14(ADC0 channel 14)
PMC17	27	I/O	Default:ADC0_CH15(ADC0 channel 15)
PMD0	2	I/O	GPIO
PMD1	1	I/O	GPIO
PMD2	46	I/O	Default:ADC1_CH2(ADC1 channel 2)
PMD3	45	I/O	Default:ADC1_CH3(ADC1 channel 3)
PMD4	44	I/O	Default:ADC1_CH6(ADC1 channel 6)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMD5	24	I/O	GPIO
PMD6	23	I/O	Default:COMP0_IN7(COMP0 channel 7)
PMD7	22	I/O	Default:COMP0_IN6(COMP0 channel 6)
PMD15	15	I/O	GPIO
PMD16	14	I/O	GPIO
PME0	60	I/O	GPIO
PME1	59	I/O	GPIO
PME2	54	I/O	Default:ADC1_CH10(ADC1 channel 10)
PME3	13	I/O	GPIO
PME4	6	I/O	GPIO
PME5	5	I/O	GPIO
PME6	53	I/O	Default:ADC1_CH11(ADC1 channel 11)
PME7	39	I/O	GPIO
PME8	17	I/O	COMP0_IN3(COMP0 channel 3)
PME9	16	I/O	GPIO
PME10	4	I/O	GPIO
PME11	3	I/O	GPIO
VREFH	9	I	AD Reference Voltage
VDDA	8	I	Analog voltage,peripheral connection with VDD
VDD	7/41	I	Power supply voltage,peripheral connection
VSS	10/40	G	GND,peripheral connection

Figure 3 100-Pin LQFP Top View

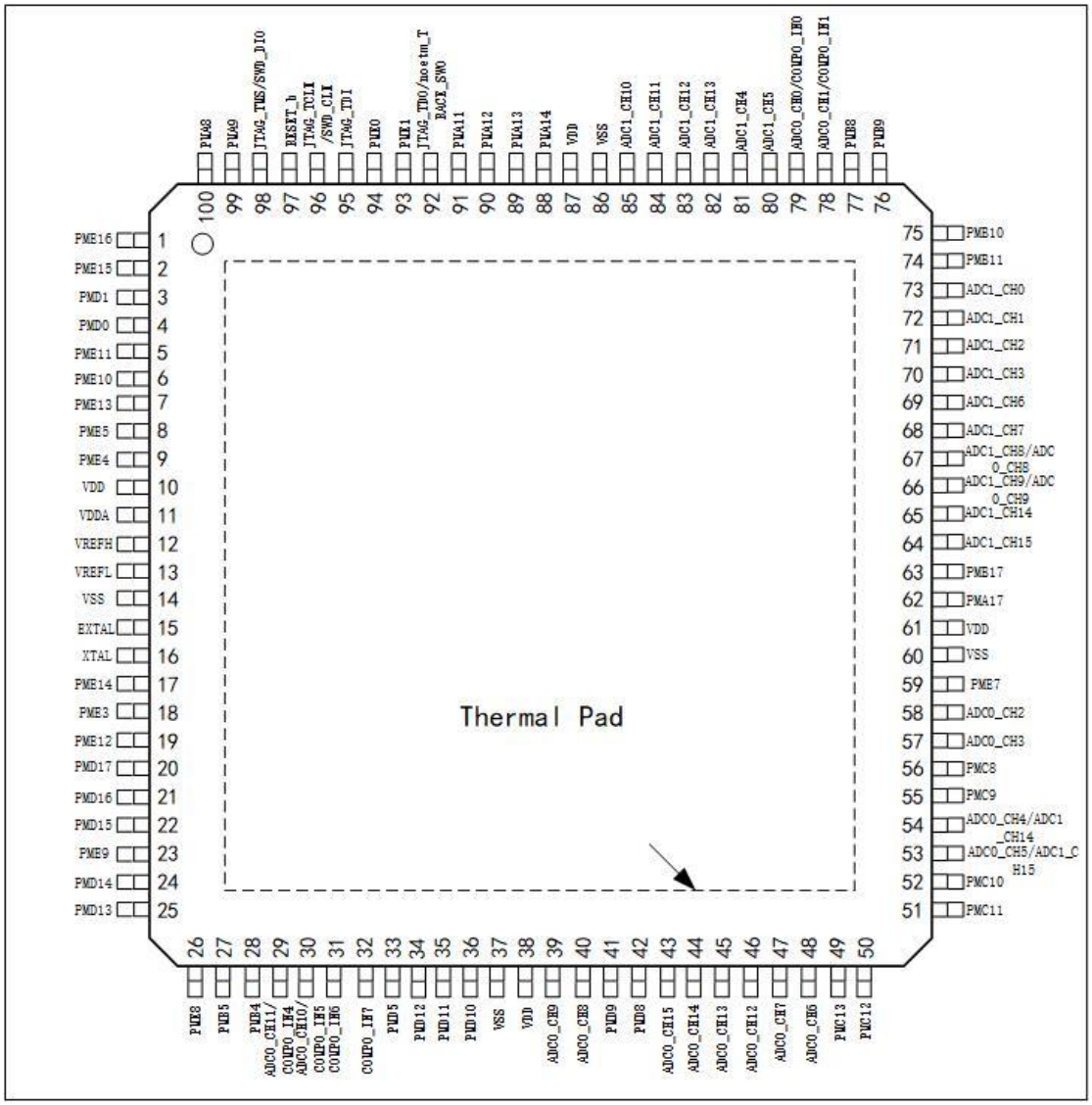


Table 3 Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA0	79	I/O	Default:ADC0_CH0/COMP0_IN0(ADC0channel0/COMP0 input channel0)
PMA1	78	I/O	Default:ADC0_CH1/COMP0_IN1(ADC0channel1/COMP0 input channel1)
PMA2	73	I/O	Default:ADC1_CH0(ADC1channel0)
PMA3	72	I/O	Default:ADC1_CH1(ADC1channel1)
PMA4	98	I/O	JTAG_TMS/SWD_DIO
PMA5	97	I/O	RESET_b
PMA6	58	I/O	Default:ADC0_CH2(ADC0channel2)
PMA7	57	I/O	Default:ADC0_CH3(ADC0channel3)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMA8	100	I/O	GPIO
PMA9	99	I/O	GPIO
PMA10	92	I/O	JTAG_TDO/noetm_TRACE_SWO
PMA11	91	I/O	GPIO
PMA12	90	I/O	GPIO
PMA13	89	I/O	GPIO
PMA14	88	I/O	GPIO
PMA15	83	I/O	Default:ADC1_CH12(ADC1channel12)
PMA16	82	I/O	Default:ADC1_CH13(ADC1channel13)
PMA17	62	I/O	GPIO
PMB0	54	I/O	Default:ADC0_CH4/ADC1_CH14(ADC0 channel 4/ ADC1 channel 14)
PMB1	53	I/O	Default:ADC0_CH5/ADC1_CH15(ADC0 channel 5/ ADC1 channel 15)
PMB2	48	I/O	Default:ADC0_CH6(ADC0channel6)
PMB3	47	I/O	Default:ADC0_CH7(ADC0channel7)
PMB4	28	I/O	GPIO
PMB5	27	I/O	GPIO
PMB6	16	I/O	XTAL
PMB7	15	I/O	EXTAL
PMB8	77	I/O	GPIO
PMB9	76	I/O	GPIO
PMB10	75	I/O	GPIO
PMB11	74	I/O	GPIO
PMB12	68	I/O	Default:ADC1_CH7(ADC1channel7)
PMB13	67	I/O	Default:ADC1_CH8/ADC0_CH8(ADC1channel8/ADC0channel8)
PMB14	66	I/O	Default:ADC1_CH9/ADC0_CH9(ADC1channel9/ADC0channel9)
PMB15	65	I/O	Default:ADC1_CH14(ADC1channel14)
PMB16	64	I/O	Default:ADC1_CH15(ADC1channel15)
PMB17	63	I/O	GPIO
PMC0	40	I/O	Default:ADC0_CH8(ADC0channel8)
PMC1	39	I/O	Default:ADC0_CH9(ADC0channel9)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMC2	30	I/O	Default:ADC0_CH10/COMP0_IN5(ADC0channel10/COMP0channel5)
PMC3	29	I/O	Default:ADC0_CH11/COMP0_IN4(ADC0channel11/COMP0channel4)
PMC4	96	I/O	JTAG_TCLK/SWD_CLK
PMC5	95	I/O	JTAG_TDI
PMC6	81	I/O	Default:ADC1_CH4(ADC1channel4)
PMC7	80	I/O	Default:ADC1_CH5(ADC1channel5)
PMC8	56	I/O	GPIO
PMC9	55	I/O	GPIO
PMC10	52	I/O	GPIO
PMC11	51	I/O	GPIO
PMC12	50	I/O	GPIO
PMC13	49	I/O	GPIO
PMC14	46	I/O	Default:ADC0_CH12(ADC0channel12)
PMC15	45	I/O	Default:ADC0_CH13(ADC0channel13)
PMC16	44	I/O	Default:ADC0_CH14(ADC0channel14)
PMC17	43	I/O	Default:ADC0_CH15(ADC0channel15)
PMD0	4	I/O	GPIO
PMD1	3	I/O	GPIO
PMD2	71	I/O	Default:ADC1_CH2(ADC1channel2)
PMD3	70	I/O	Default:ADC1_CH3(ADC1channel3)
PMD4	69	I/O	Default:ADC1_CH6(ADC1channel6)
PMD5	33	I/O	GPIO
PMD6	32	I/O	Default:COMP0_IN7(COMP0channel7)
PMD7	31	I/O	Default:COMP0_IN6(COMP0channel6)
PMD8	42	I/O	GPIO
PMD9	41	I/O	GPIO
PMD10	36	I/O	GPIO
PMD11	35	I/O	GPIO
PMD12	34	I/O	GPIO
PMD13	25	I/O	GPIO

PIN		TYPE	DESCRIPTION
NAME	NO.		
PMD14	24	I/O	GPIO
PMD15	22	I/O	GPIO
PMD16	21	I/O	GPIO
PMD17	20	I/O	GPIO
PME0	94	I/O	GPIO
PME1	93	I/O	GPIO
PME2	85	I/O	Default:ADC1_CH10(ADC1channel10)
PME3	18	I/O	GPIO
PME4	9	I/O	GPIO
PME5	8	I/O	GPIO
PME6	84	I/O	Default:ADC1_CH11(ADC1channel11)
PME7	59	I/O	GPIO
PME8	26	I/O	COMP0_IN3(COMP0 channel 3)
PME9	23	I/O	GPIO
PME10	6	I/O	GPIO
PME11	5	I/O	GPIO
PME12	19	I/O	GPIO
PME13	7	I/O	GPIO
PME14	17	I/O	GPIO
PME15	2	I/O	GPIO
PME16	1	I/O	GPIO
VREFH	12	I	AD Reference Voltage
VDDA	11	I	Analog voltage,peripheral connection with VDD
VDD	10/38/61/87	I	Power supply voltage,peripheral connection
VREFL	13	G	AD Reference GND
VSS	86/60/37/14	G	GND,peripheral connection

5 Pin Multiplexing

Table 4 Pin Multiplexing

G32A1445		GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64pin LQFP	100pin LQFP									
-	1	PME16	-	PME16	LPUART1_RTS	LPSPI2_SIN	FTMR2_CH7	-	FXCOM_D3	TMC_OUT7
-	2	PME15	-	PME15	LPUART1_CTS	LPSPI2_SCK	FTMR2_CH6	-	FXCOM_D2	TMC_OUT6
1	3	PMD1	-	PMD1	FTMR0_CH3	LPSPI1_SIN	FTMR2_CH1	-	FXCOM_D1	TMC_OUT2
2	4	PMD0	-	PMD0	FTMR0_CH2	LPSPI1_SCK	FTMR2_CH0	-	FXCOM_D0	TMC_OUT1
3	5	PME11	-	PME11	LPSPI2_PCS0	LPTMR0_ALT1	FTMR2_CH5	-	FXCOM_D5	TMC_OUT5
4	6	PME10	-	PME10	CLKOUT	LPSPI2_PCS1	FTMR2_CH4	-	FXCOM_D4	TMC_OUT4
-	7	PME13	-	PME13	-	LPSPI2_PCS2	FTMR2_FLT0	-	-	-
5	8	PME5	-	PME5	TCLK2	FTMR2_QD_PHA	FTMR2_CH3	CAN0_TX	FXCOM_D7	EWDT_IN
6	9	PME4	-	PME4	-	FTMR2_QD_PHB	FTMR2_CH2	CAN0_RX	FXCOM_D6	EWDT_OUT_b
7	10	VDD	VDD	-	-	-	-	-	-	-
8	11	VDDA	VDDA	-	-	-	-	-	-	-
9	12	VREFH	VREFH	-	-	-	-	-	-	-
-	13	VREFL	VREFL	-	-	-	-	-	-	-
10	14	VSS	VSS	-	-	-	-	-	-	-
11	15	PMB7	EXTAL	PMB7	LPI2C0_SCL	-	-	-	-	-
12	16	PMB6	XTAL	PMB6	LPI2C0_SDA	-	-	-	-	-
-	17	PME14	-	PME14	FTMR0_FLT1	-	FTMR2_FLT1	-	-	-

G32A1445		GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64pin LQFP	100pin LQFP									
13	18	PME3	-	PME3	FTMR0_FLT0	LPUART2_RTS	FTMR2_FLT0	-	TMC_IN6	COMP0_OUT
-	19	PME12	-	PME12	FTMR0_FLT3	LPUART2_TX	-	-	-	-
-	20	PMD17	-	PMD17	FTMR0_FLT2	LPUART2_RX	-	-	-	-
14	21	PMD16	-	PMD16	FTMR0_CH1	-	LPSPI0_SIN	COMP0_RRT	-	-
15	22	PMD15	-	PMD15	FTMR0_CH0	-	LPSPI0_SCK	-	-	-
16	23	PME9	-	PME9	FTMR0_CH7	LPUART2_CTS	-	-	-	-
-	24	PMD14	-	PMD14	FTMR2_CH5	LPUART1_TX	-	-	-	CLKOUT
-	25	PMD13	-	PMD13	FTMR2_CH4	LPUART1_RX	-	-	-	RTC_CLKOUT
17	26	PME8	COMP0_IN3	PME8	FTMR0_CH6	-	-	-	-	-
18	27	PMB5	-	PMB5	FTMR0_CH5	LPSPI0_PCS1	LPSPI0_PCS0	CLKOUT	TMC_IN0	-
19	28	PMB4	-	PMB4	FTMR0_CH4	LPSPI0_SOUT	-	-	TMC_IN1	-
20	29	PMC3	ADC0_CH11/ COMP0_IN4	PMC3	FTMR0_CH3	CAN0_TX	LPUART0_TX	-	-	-
21	30	PMC2	ADC0_CH10/ COMP0_IN5	PMC2	FTMR0_CH2	CAN0_RX	LPUART0_RX	-	-	-
22	31	PMD7	COMP0_IN6	PMD7	LPUART2_TX	-	FTMR2_FLT3	-	-	-
23	32	PMD6	COMP0_IN7	PMD6	LPUART2_RX	-	FTMR2_FLT2	-	-	-
24	33	PMD5	-	PMD5	FTMR2_CH3	LPTMR0_ALT2	FTMR2_FLT1	-	TMC_IN7	-
-	34	PMD12	-	PMD12	FTMR2_CH2	-	-	-	LPUART2_RTS	-
-	35	PMD11	-	PMD11	FTMR2_CH1	FTMR2_QD_PHA	-	-	LPUART2_CTS	-

G32A1445		GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64pin LQFP	100pin LQFP									
-	36	PMD10	-	PMD10	FTMR2_CH0	FTMR2_QD_PHB	-	-	-	-
40	37	VSS	VSS	-	-	-	-	-	-	-
-	38	VDD	VDD	-	-	-	-	-	-	-
25	39	PMC1	ADC0_CH9	PMC1	FTMR0_CH1	LPSPI2_SOUT	-	-	FTMR1_CH7	-
26	40	PMC0	ADC0_CH8	PMC0	FTMR0_CH0	LPSPI2_SIN	-	-	FTMR1_CH6	-
-	41	PMD9	-	PMD9	-	FXCOM_D0	FTMR2_FLT3	-	FTMR1_CH5	-
-	42	PMD8	-	PMD8	-	-	FTMR2_FLT2	FXCOM_D1	FTMR1_CH4	-
27	43	PMC17	ADC0_CH15	PMC17	FTMR1_FLT3	CAN2_TX	-	-	-	-
28	44	PMC16	ADC0_CH14	PMC16	FTMR1_FLT2	CAN2_RX	-	-	-	-
29	45	PMC15	ADC0_CH13	PMC15	FTMR1_CH3	LPSPI2_SCK	-	-	TMC_IN8	-
30	46	PMC14	ADC0_CH12	PMC14	FTMR1_CH2	LPSPI2_PCS0	-	-	TMC_IN9	-
31	47	PMB3	ADC0_CH7	PMB3	FTMR1_CH1	LPSPI0_SIN	FTMR1_QD_PHA	-	TMC_IN2	-
32	48	PMB2	ADC0_CH6	PMB2	FTMR1_CH0	LPSPI0_SCK	FTMR1_QD_PHB	-	TMC_IN3	-
-	49	PMC13	-	PMC13	FTMR3_CH7	FTMR2_CH7	LPUART2_RTS	-	-	-
-	50	PMC12	-	PMC12	FTMR3_CH6	FTMR2_CH6	LPUART2_CTS	-	-	-
-	51	PMC11	-	PMC11	FTMR3_CH5	-	-	-	TMC_IN10	-
-	52	PMC10	-	PMC10	FTMR3_CH4	-	-	-	TMC_IN11	-
33	53	PMB1	ADC0_CH5/ADC1_CH15	PMB1	LPUART0_TX	LPSPI0_SOUT	TCLK0	CAN0_TX	-	-

G32A1445		GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64pin LQFP	100pin LQFP									
34	54	PMB0	ADC0_CH4/ADC1_CH14	PMB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ALT3	CAN0_RX	-	-
35	55	PMC9	-	PMC9	LPUART1_TX	FTMR1_FLT1	-	-	LPUART0_RTS	-
36	56	PMC8	-	PMC8	LPUART1_RX	FTMR1_FLT0	-	-	LPUART0_CTS	-
37	57	PMA7	ADC0_CH3	PMA7	FTMR0_FLT2	-	RTC_CLKIN	-	LPUART1_RTS	-
38	58	PMA6	ADC0_CH2	PMA6	FTMR0_FLT1	LPSPI1_PCS1	-	-	LPUART1_CTS	-
39	59	PME7	-	PME7	FTMR0_CH7	FTMR3_FLT0	-	-	-	-
-	60	VSS	VSS	-	-	-	-	-	-	-
41	61	VDD	VDD	-	-	-	-	-	-	-
-	62	PMA17	-	PMA17	FTMR0_CH6	FTMR3_FLT0	EWDT_OUT_b	-	-	-
-	63	PMB17	-	PMB17	FTMR0_CH5	LPSPI1_PCS3	-	-	-	-
-	64	PMB16	ADC1_CH15	PMB16	FTMR0_CH4	LPSPI1_SOUT	-	-	-	-
-	65	PMB15	ADC1_CH14	PMB15	FTMR0_CH3	LPSPI1_SIN	-	-	-	-
-	66	PMB14	ADC1_CH9/ADC0_CH9	PMB14	FTMR0_CH2	LPSPI1_SCK	-	-	-	-
42	67	PMB13	ADC1_CH8/ADC0_CH8	PMB13	FTMR0_CH1	FTMR3_FLT1	CAN2_TX	-	-	-
43	68	PMB12	ADC1_CH7	PMB12	FTMR0_CH0	FTMR3_FLT2	CAN2_RX	-	-	-
44	69	PMD4	ADC1_CH6	PMD4	FTMR0_FLT3	FTMR3_FLT3	-	-	-	-
45	70	PMD3	ADC1_CH3	PMD3	FTMR3_CH5	LPSPI1_PCS0	FXCOM_D5	FXCOM_D7	TMC_IN4	NMI_b
46	71	PMD2	ADC1_CH2	PMD2	FTMR3_CH4	LPSPI1_SOUT	FXCOM_D4	FXCOM_D6	TMC_IN5	-
47	72	PMA3	ADC1_CH1	PMA3	FTMR3_CH1	LPI2C0_SCL	EWDT_IN	FXCOM_D5	LPUART0_TX	-

G32A1445		GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64pin LQFP	100pin LQFP									
48	73	PMA2	ADC1_CH0	PMA2	FTMR3_CH0	LPI2C0_SDA	EWDT_OUT_b	FXCOM_D4	LPUART0_RX	-
-	74	PMB11	-	PMB11	FTMR3_CH3	LPI2C0_HREQ	-	-	-	-
-	75	PMB10	-	PMB10	FTMR3_CH2	LPI2C0_SDAS	-	-	-	-
-	76	PMB9	-	PMB9	FTMR3_CH1	LPI2C0_SCLS	-	-	-	-
-	77	PMB8	-	PMB8	FTMR3_CH0	-	-	-	-	-
49	78	PMA1	ADC0_CH1/COMP0_IN1	PMA1	FTMR1_CH1	LPI2C0_SDAS	FXCOM_D3	FTMR1_QD_PHA	LPUART0_RTS	TMC_OUT0
50	79	PMA0	ADC0_CH0/COMP0_IN0	PMA0	FTMR2_CH1	LPI2C0_SCLS	FXCOM_D2	FTMR2_QD_PHA	LPUART0_CTS	TMC_OUT3
51	80	PMC7	ADC1_CH5	PMC7	LPUART1_TX	CAN1_TX	FTMR3_CH3	-	FTMR1_QD_PHA	-
52	81	PMC6	ADC1_CH4	PMC6	LPUART1_RX	CAN1_RX	FTMR3_CH2	-	FTMR1_QD_PHB	-
-	82	PMA16	ADC1_CH13	PMA16	FTMR1_CH3	LPSPI1_PCS2	-	-	-	-
-	83	PMA15	ADC1_CH12	PMA15	FTMR1_CH2	LPSPI0_PCS3	LPSPI2_PCS3	-	-	-
53	84	PME6	ADC1_CH11	PME6	LPSPI0_PCS2	-	FTMR3_CH7	-	LPUART1_RTS	-
54	85	PME2	ADC1_CH10	PME2	LPSPI0_SOUT	LPTMR0_ALT3	FTMR3_CH6	-	LPUART1_CTS	-
-	86	VSS	VSS	-	-	-	-	-	-	-
-	87	VDD	VDD	-	-	-	-	-	-	-
-	88	PMA14	-	PMA14	FTMR0_FLT0	FTMR3_FLT1	EWDT_IN	-	FTMR1_FLT0	-
55	89	PMA13	-	PMA13	FTMR1_CH7	CAN1_TX	-	-	FTMR2_QD_PHA	-

G32A1445		GPIO	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
64pin LQFP	100pin LQFP									
56	90	PMA12	-	PMA12	FTMR1_CH6	CAN1_RX	-	-	FTMR2_QD_PHB	-
57	91	PMA11	-	PMA11	FTMR1_CH5	-	FXCOM_D1	COMP0_RRT	-	-
58	92	PMA10	-	PMA10	FTMR1_CH4	-	FXCOM_D0	-	-	JTAG_TDO/noetm_TRACE_SWO
59	93	PME1	-	PME1	LPSPI0_SIN	LPI2C0_HREQ	-	LPSPI1_PCS0	FTMR1_FLT1	-
60	94	PME0	-	PME0	LPSPI0_SCK	TCLK1	-	LPSPI1_SOUT	FTMR1_FLT2	-
61	95	PMC5	-	PMC5	FTMR2_CH0	RTC_CLKOUT	-	-	FTMR2_QD_PHB	JTAG_TDI
62	96	PMC4	COMP0_IN2	PMC4	FTMR1_CH0	RTC_CLKOUT	-	EWDT_IN	FTMR1_QD_PHB	JTAG_TCLK/SWD_CLK
63	97	PMA5	-	PMA5	-	TCLK1	-	-	-	RESET_b
64	98	PMA4	-	PMA4	-	-	COMP0_OUT	EWDT_OUT_b	-	JTAG_TMS/SWD_DIO
-	99	PMA9	-	PMA9	LPUART2_TX	LPSPI2_PCS0	FXCOM_D7	FTMR3_FLT2	FTMR1_FLT3	-
-	100	PMA8	-	PMA8	LPUART2_RX	LPSPI2_SOUT	FXCOM_D6	FTMR3_FLT3	-	-

6 Electrical Characteristics

6.1 Test under general operating conditions

6.1.1 Absolute maximum rated value

If the load on the device exceeds the absolute maximum rated value, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and it cannot be ensured that the device functions normally under this condition. At the same time, operation shall be performed strictly according to all the conditions defined in the table, and violating any one or more conditions cannot guarantee normal operation of the function.

Unless otherwise specified, all maximum and minimum values can support the full voltage and temperature range.

Table 5 Absolute Maximum Ratings

Symbol	Parameter (1)	Minimum value	Typical value	Maximum value	Unit
T_A(2)	Ambient temperature	-40	-	125	℃
T_{STG}	Storage temperature range	-55	-	165	
I_{INJ}(3)	Continuous DC input current(positive/negative) for injection into I/O pins	-3	-	+3	mA
$\Sigma\|I_{INJ}\|$	Total injection current of all pins (continuous DC limit)	-	-	30	
V_{DD}(4)	2.7V~5.5V input power supply voltage	-0.3	-	5.8(5)	V
V_{REFH}	3.3V/5.0V ADC high reference voltage	-0.3	-	5.8(5)	
V_{IN}	Continuous DC voltage on any I/O pin relative to V_{SS}	-0.8	-	5.8(6)	
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pins exceeds the V_{IN} limit	-	-	6.8(7)	
T_{ramp_MCU}(8)	MCU supply rise slope	0.5V/min	-	100V/ms	-
T_{ramp}(9)	ECU supply rise slope	0.5V/min	-	500V/ms	-

Notes:

(1) Unless otherwise specified, all voltages are referred to V_{SS} ;

(2) T_J (junction temperature)=135℃. Assuming T_A=125℃ in run mode;

T_J (junction temperature)=125℃. Assuming T_A=105℃ in high-speed run mode;

Assuming the maximum of the 2s2p board is θ JA. Refer to Temperature Characteristics);

(3) When the input pad voltage is close to V_{DD} or V_{SS}, current injection cannot be conducted;

(4) When V_{DD} changes between the minimum and absolute maximum values, both I/O and ADC will change. For detailed information, please refer to the I/O parameters and ADC electrical specifications;

(5) When the lifespan is 60 seconds: unlimited, that is, this part is not held in a reset state and can be switched;

When the service life is 10 hours: this part is held in the reset state through external circuits, and cannot be switched;

When operating with a power supply between 5.5V and 5.8V not in reset state, a total of 60 seconds is allowed, but this part will run with reduced function;

When operating with a power supply between 5.5V and 5.8V while the system is held in the reset state through external circuit, a total of 10 hours is allowed;

All power supplies shall be always maintained within the given working conditions, and once they deviate from the working conditions, the equipment shall be reset or powered off. If the given time or power supply voltage limit is exceeded, permanent damage might be caused to the equipment;

(6) Obey the maximum current injection limit.

(7) Under the condition of 60-second lifespan; the equipment is in a reset state (no output enabled/switched);

(8) The supply rise slope of the electronic control unit (ECU) under typical operating conditions and absolute maximum slope;

(9) The supply rise slope of MCU under typical operating conditions and absolute maximum slope.

6.1.2 Voltage and current operation requirements

The functionality of the equipment is guaranteed above the LVR level, but when the voltage is below 2.7V, the electrical performance of the ADC, COMP, IO, and communication modules will correspondingly decrease.

Table 6 Electrical Characteristics of Voltage and Current (1)

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
V_{DD}(2) (3)	Supply voltage	2.7(4)	-	5.5	V
V_{DDA}(3)	Analog power supply voltage	2.7	-	5.5	
V_{DD} -V_{DDA}(3)	V_{DD}-V_{DDA} voltage difference	-0.1	-	0.1	
V_{ODPU}(5)	Open-drain pull-up voltage	V_{DD}	-	V_{DD}	
$V_{DD(OFF)}$	The voltage allowed to be generated on the VDD pin when the VDD is not powered by any external power supply	0	-	0.1	
I_{INJ}(6)	Injection current of I/O pin (continuous DC)	-3	-	+3	mA
ΣI_{INJ_OP}	The total injection current (continuous DC) of all I/O pins, in order not to reduce the accuracy of the analog module: ADC and ACOMP (refer to the "Analog Module" section)	-	-	30	

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$V_{REFINTL}$	Low level of ADC built-in reference voltage	-0.1	-	0.1	V
$V_{REFINTH}$(7)	High level of ADC built-in reference voltage	2.7	-	V_{DDA}+0.1	

Notes:

(1) Unless otherwise specified, the data in the table is tested with the typical silicon process under the conditions of T_A=25℃ and V_{DD}=V_{DDA}=V_{REFH}=5V.

(2) The analog characteristics of I/O and ADC will change with the change of V_{DD} between the minimum and maximum values.

(3) VDD and VDDA must be shorted to the common power supply on the PCB. The differential voltage between V_{DD} and V_{DDA} is only used for RF-AC. Select a suitable decoupling capacitor to filter the noise on the power supply.

(4) When executing from internal HSICLK, it will work at 2.7V in all modes

(5) The open-drain output must be pulled to V_{DD}.

(6) When the input pad voltage is close to V_{DD} or V_{SS}, current injection cannot be conducted.

(7) $V_{REFINTH}$ should always be ≤ V_{DDA}+0.1 V and V_{DD}+0.1 V.

6.1.3 Temperature operation characteristics

Table 7 Temperature Operation Characteristics

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$T_{A(MGP)}$	Ambient temperature under bias conditions	≤80 MHz,RUN mode	-40	-	125	℃
$T_{J(MGP)}$	Junction temperature under bias conditions	≤80 MHz,RUN mode	-40	-	135	
$T_{A(CGP)}$	Ambient temperature under bias conditions	≤112 MHz,HSR mode	-40	-	85	
$T_{J(CGP)}$	Junction temperature under bias conditions	≤112 MHz,HSR mode	-40	-	105	
$T_{A(VGP)}$	Ambient temperature under bias conditions	≤112 MHz,HSR mode	-40	-	105	
$T_{J(VGP)}$	Junction temperature under bias conditions	≤112 MHz,HSR mode	-40	-	125	

6.1.4 Power supply and ground pins

Figure 4 LQFP64 Encapsulation Outgoing Line Separate Decoupling

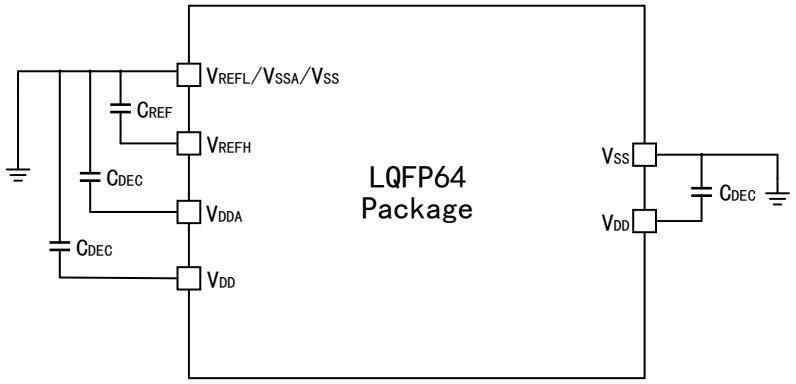
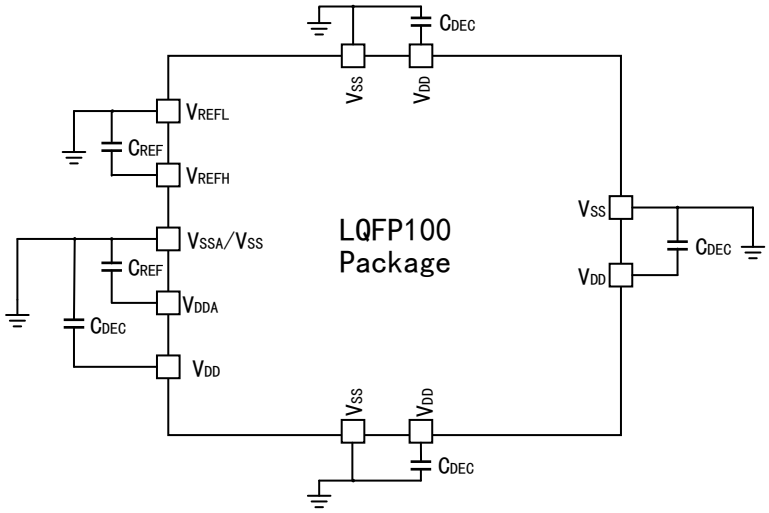


Figure 5 LQFP100 Encapsulation Outgoing Line Separate Decoupling



Note: V_{DD} and V_{DDA} must be shorted to the common power supply on the PCB

Table 8 Decoupling capacitor (1) (2)

Symbol	Parameter	Minimum value(3)	Typical value	Maximum value	Unit
C_{DEC}(4) (6) (7)	Decoupling capacitance	70	100	-	nF
C_{REFINT}(4) (5)	ADC built-in reference high decoupling capacitance	70	100	-	

Notes:

(1) V_{DD} and V_{DDA} must be shorted to the common power supply on the PCB. The differential voltage between V_{DD} and V_{DDA} is only used for RF-AC. Select a suitable decoupling capacitor to filter the noise on the power supply.

(2) All V_{SS} pins should be connected to a PCB-level common ground.

(3) Low-ESR ceramic capacitor (e.g. X7R type) shall be selected as decoupling capacitor.

(4) Recommended minimum value while considering the component aging and tolerance.

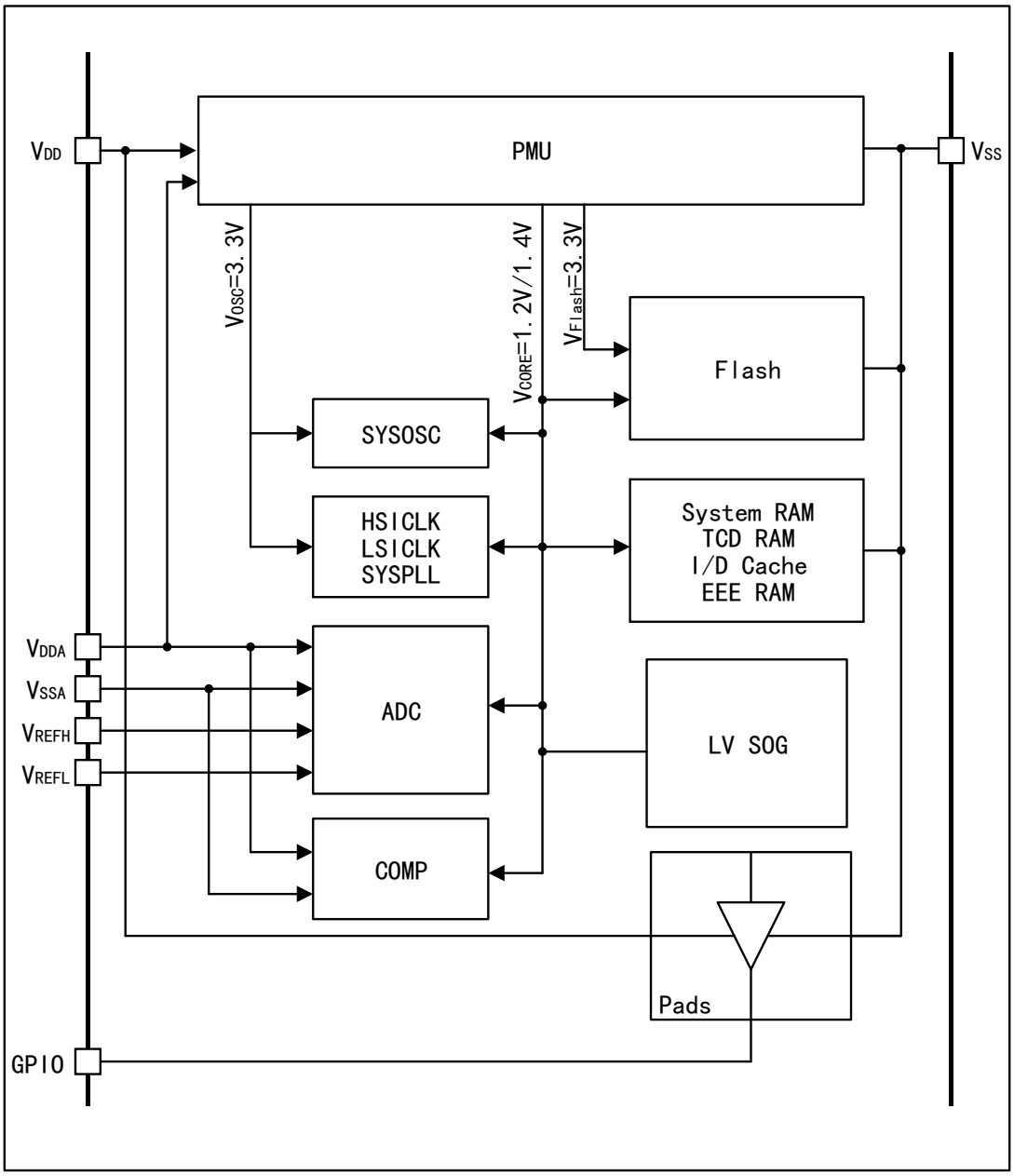
(5) All decoupling capacitors shall be as close as possible to the corresponding power supply and ground pin.

(6) To improve the performance, it is recommended to use 0.1μF, 10μF and 1 nF capacitors in parallel.

(7) The filtering of decoupling device power supply must comply with the following best practice rules:

- The grounding of the protective device and the grounding plane under the integrated circuit shall be connected as short as possible.
- The length of the trace from the protective device to the trace or to the ground shall not exceed 1 mm.
- The protective/decoupling capacitor must be located on the trace path connected to the component.
- The protective/decoupling capacitor must be as close to the input pin of the equipment as possible (at most 2 mm).

Figure 6 Power Supply Scheme



6.1.5 Power mode conversion characteristics

All specifications in the table below use this clock configuration

Table 9 Clock Configuration

Mode	Clock configuration	
RUN mode	Clock Source	HSICLK
	SYS_CLK/CORE_CLK	48MHz
	BUS_CLK	48MHz
	FLASH_CLK	24MHz
HSR mode	Clock Source	SYSPLL
	SYS_CLK/CORE_CLK	112MHz
	BUS_CLK	56MHz
	FLASH_CLK	28MHz
VLPR mode	Clock Source	LSICLK
	SYS_CLK/CORE_CLK	4MHz
	BUS_CLK	4MHz
	FLASH_CLK	1MHz
STOP1/STOP2 mode	Clock Source	HSICLK
	SYS_CLK/CORE_CLK	48MHz
	BUS_CLK	48MHz
	FLASH_CLK	24MHz
VLPS mode	Disable all clock sources (1)	

Note: (1) It refers to HSICLK/SYSOSC/SYSPLL

Table 10 Power Mode Conversion Operation Behavior

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
t_{POR}	The time required to execute the first command from V_{DD} to 2.7V within the operating temperature range of the chip after the power-on reset event occurs.	-	325	-	μs
	RUN→STOP1	0.35	0.38	0.4	μs
	RUN→STOP2	0.2	0.23	0.25	μs
	RUN→VLPS	0.3	0.35	0.4	μs
	RUN→VLPR	3.5	3.8	5	μs
	RUN→Compute operation	0.72	0.75	0.77	μs
	HSR(1) →Compute operation	0.3	0.31	0.35	μs
	VLPS→RUN	8	-	17	μs
	VLPS→VLPR	18.8	23	27.75	μs

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
	VLPS→Asynchronous DMA Wake-up	105	110	125	μs
	VLPR→VLPS	5.1	5.7	6.5	μs
	VLPR→RUN	19	-	26	μs
	STOP1→RUN	0.07	0.075	0.08	μs
	STOP2→RUN	0.07	0.075	0.08	μs
	STOP1→Asynchronous DMA Wake-up	1	1.1	1.3	μs
	STOP2→Asynchronous DMA Wake-up	1	1.1	1.3	μs
	Pin reset→Code execution	-	214	-	μs

Note: (1) HSR mode shall only be used when it is necessary to use frequency exceeding 80 MHz. When using a frequency of 80 MHz and below, it is recommended to use the RUN mode.

6.1.6 ESD and Latch-up protection characteristics

Table 11 ESD Electrostatic Discharge Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model) (1)	-4000	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging device model) (1)			
	All pins except corner pins	-500	500	V
	Corner pin	-750	750	V

Note: (1) Equipment fault is defined as: "Once the equipment is exposed to ESD pulses, the equipment will not meet the specification requirements."

Table 12 Latch-up Static Latch Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
LU	Latch-up current at T_A=125℃	-100	100	mA

6.2 Temperature characteristics

6.2.1 General precautions for specifications at maximum junction temperature

Calculation of chip junction temperature T_J can be obtained from the following equation:

$$T_J = (R_{\theta JA} \times P_D) + T_A$$

Where: $R_{\theta JA}$ represents the thermal resistance of the joint to the environment

(℃/W), P_D represents the power dissipation of the package (W), and T_A represents the ambient temperature of the packaging (℃).

The thermal resistance connected to the environment is an industry standard value, and can be used to estimate the temperature characteristics quickly and conveniently. Usually it is determined by two values: the determined of the single-layer boards and the value measured on the double-layer boards. Which value is closer to the application depends on the power consumed by other components on the board. The values on the single-layer boards are applicable to tightly encapsulated printed circuit boards; if the power consumption of the board is low and the components are well separated, the value obtained on the board with an internal plane is more suitable.

When using a radiator, the thermal resistance in the following equation is expressed as the sum of the thermal resistance connected to the shell and the ambient thermal resistance:

$$R_{\theta JA} = R_{\theta CA} + R_{\theta JC}$$

Where: $R_{\theta JA}$ represents the thermal resistance (℃/W) of the joint to the environment, $R_{\theta CA}$ represents ambient thermal resistance (℃/W), and $R_{\theta JC}$ represents the thermal resistance (℃/W) of the joint to the shell.

The value of $R_{\theta JC}$ is related to the equipment and is not controlled by users. Users can change the instance to the ambient thermal resistance $R_{\theta CA}$ by controlling the thermal environment. For example, users can change the heat dissipation of the printed circuit board around the equipment, the airflow around the equipment, interface materials, wiring on the printed circuit board, or dimensions of the radiator.

When the radiator is not used, the thermal characterization parameters (ψ_{JT}) can be used to determine the junction temperature of the device in the application, and the following equation can be used to measure the center temperature at the top of the package shell:

$$T_J=T_T+(\psi_{JT}\times P_D)$$

Where: T_T represents the temperature of the thermocouple at the top of the package (℃), ψ_{JT} represents the thermal characterization parameter (℃/W), and P_D represents the power dissipation of the package (W).

According to the JESD51-2 standard, the temperature characteristic parameters are measured with a No. 40 T-type thermocouple connected to the center of the top of the package with epoxy resin.

Note:

(1) The thermocouple wire shall be laid flat on the package shell to avoid measurement errors caused by the cooling effect of the thermocouple wires.

(2) Ensure that the thermocouple junction is located on the package. Place a small amount of epoxy resin on the thermocouple junction and place it on the approximately 1mm wire extending from the junction.

6.2.2 Temperature characteristics

Table 13 Temperature Characteristics

Symbol	Parameter	Condition	Package		Unit
			LQFP64	LQFP100	
$R_{\theta JA}$(1)	Thermal resistance, joint to the environment (natural convection)	Single-layer board (1s)	61	52	℃/W
		Double-layer board (1s1p)	45	42	℃/W
		Four-layer board (2s2p)	43	40	℃/W
$R_{\theta JMA}$(1)	Thermal resistance, jointto the environment (forced convection, 200 feet/min)	Single-layer board (1s)	49	42	℃/W
		Double-layer board (1s1p)	38	35	℃/W
		Four-layer board (2s2p)	36	34	℃/W
$R_{\theta JC}$(2)	Thermal resistance, joint to the shell	-	12	12	℃/W
$R_{\theta JB}$(3)	Thermal resistance, joint to the board	-	25	25	℃/W
ψ_{JT}(4)	Thermal resistance, joint to the top of the package	Natural convection	2	2	℃/W

Notes:

(1) The size of tube core, thermal resistance of package, thermal resistance of board, ambient temperature, installation position (board) temperature, air flow rate, power consumption on the chip, and power consumption of other components on the board all affect the junction temperature, and the junction temperature is a function of these parameters.

(2) Indicates the thermal resistance between the mold and the surface of the shell, measured through the cold plate method.

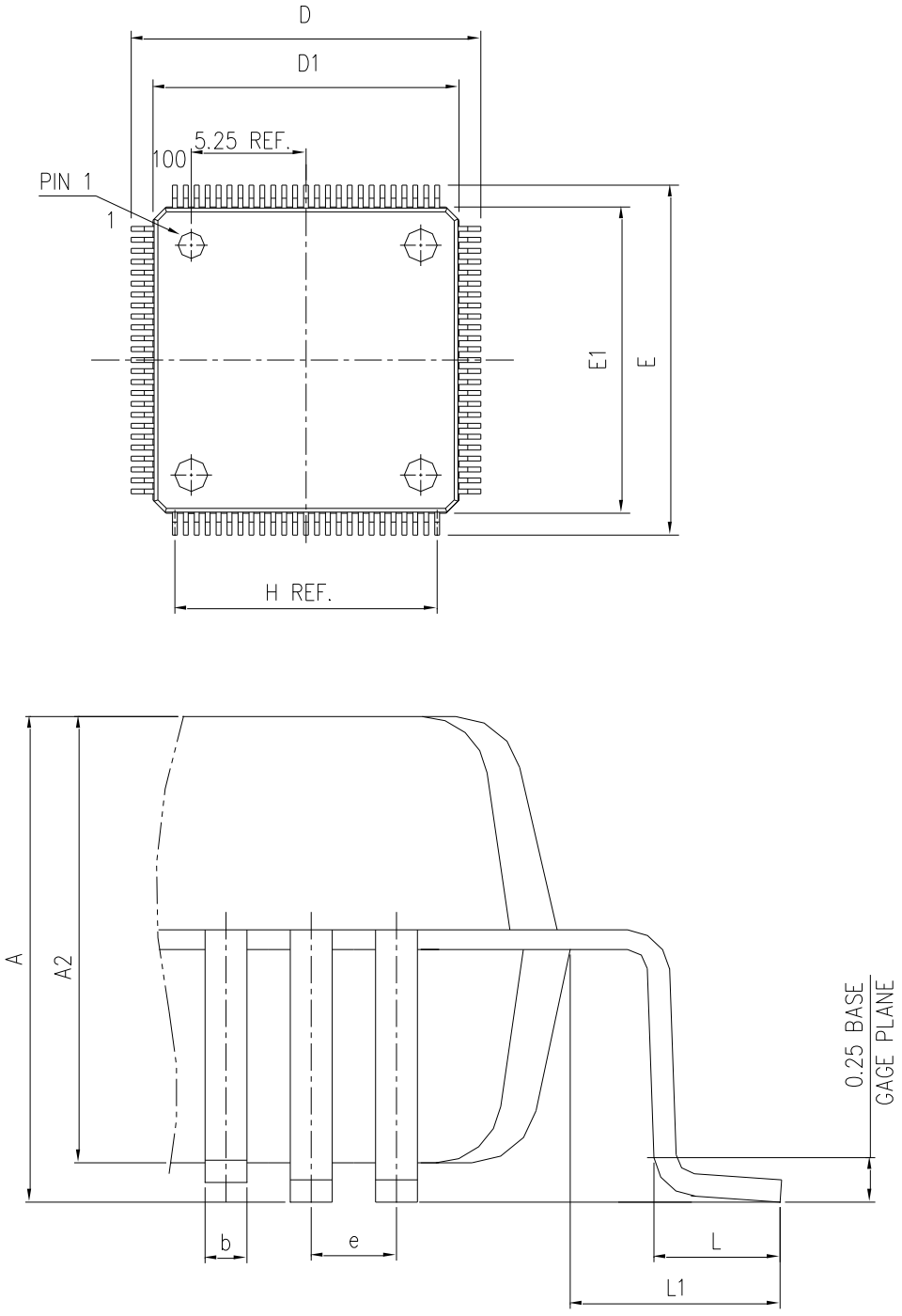
(3) Indicates the thermal resistance between the chip and the printed circuit board. The temperature of the board is measured on the top surface of the board near the package.

(4) Thermal characterization parameter, indicating the temperature difference between the junction temperature and the top of the package. When Greek alphabet is not available, this parameter will be expressed as Psi JT.

7 Package Information

7.1 LQFP100 package information

Figure 7 LQFP100 Package Diagram



(1) The figure is not drawn to scale.

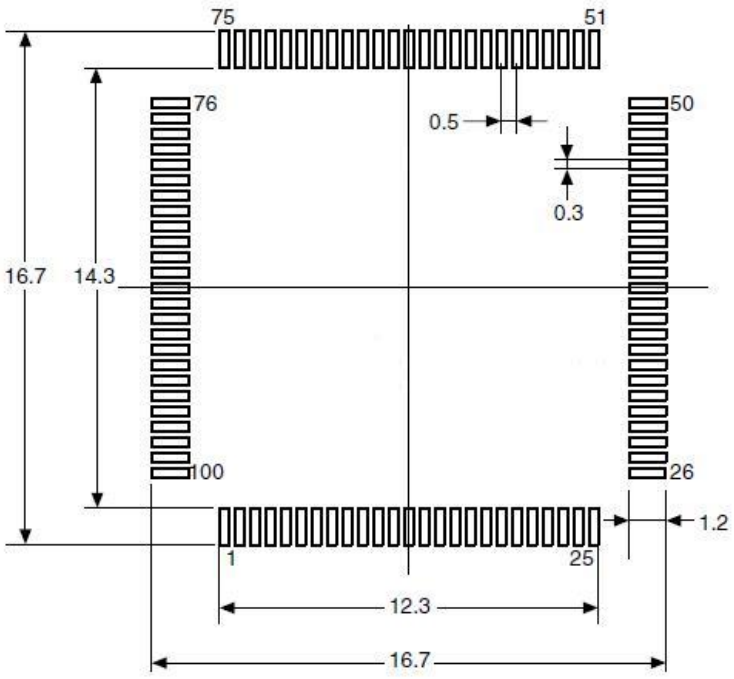
(2) All pins should be soldered to the PCB.

Table 14 LQFP100 Package Data

DIMENSION LIST（FOOTPRINT: 2.00）			
S/N	**SYM**	**DIMENDIONS**	**REMARKS**
1	A	MAX. 1.600	OVERALL HEIGHT
2	A2	1.400±0.050	PKG THICKNESS
3	D	16.000±0.200	LEAD TIP TO TIP
4	D1	14.000±0.100	PKG LENGTH
5	E	16.000±0.200	LEAD TIP TO TIP
6	E1	14.000±0.100	PKG WDTH
7	L	0.600±0.150	FOOT LENGTH
8	L1	1.000 REF	LEAD LENGTH
9	e	0.500 BASE	LEAD PITCH
10	H (REF)	(12.00)	CUM LEAD PITCH
11	b	0.22±0.050	LEAD WIDTH

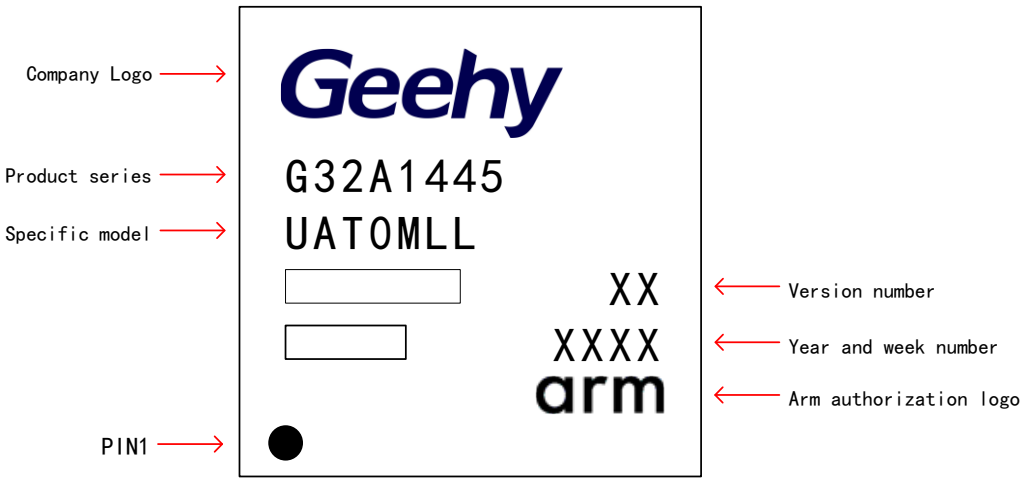
Note: Dimensions are marked in millimeters.

Figure 8 LQFP100 - 100 Pins, 14 x 14mm Welding Layout Recommendations



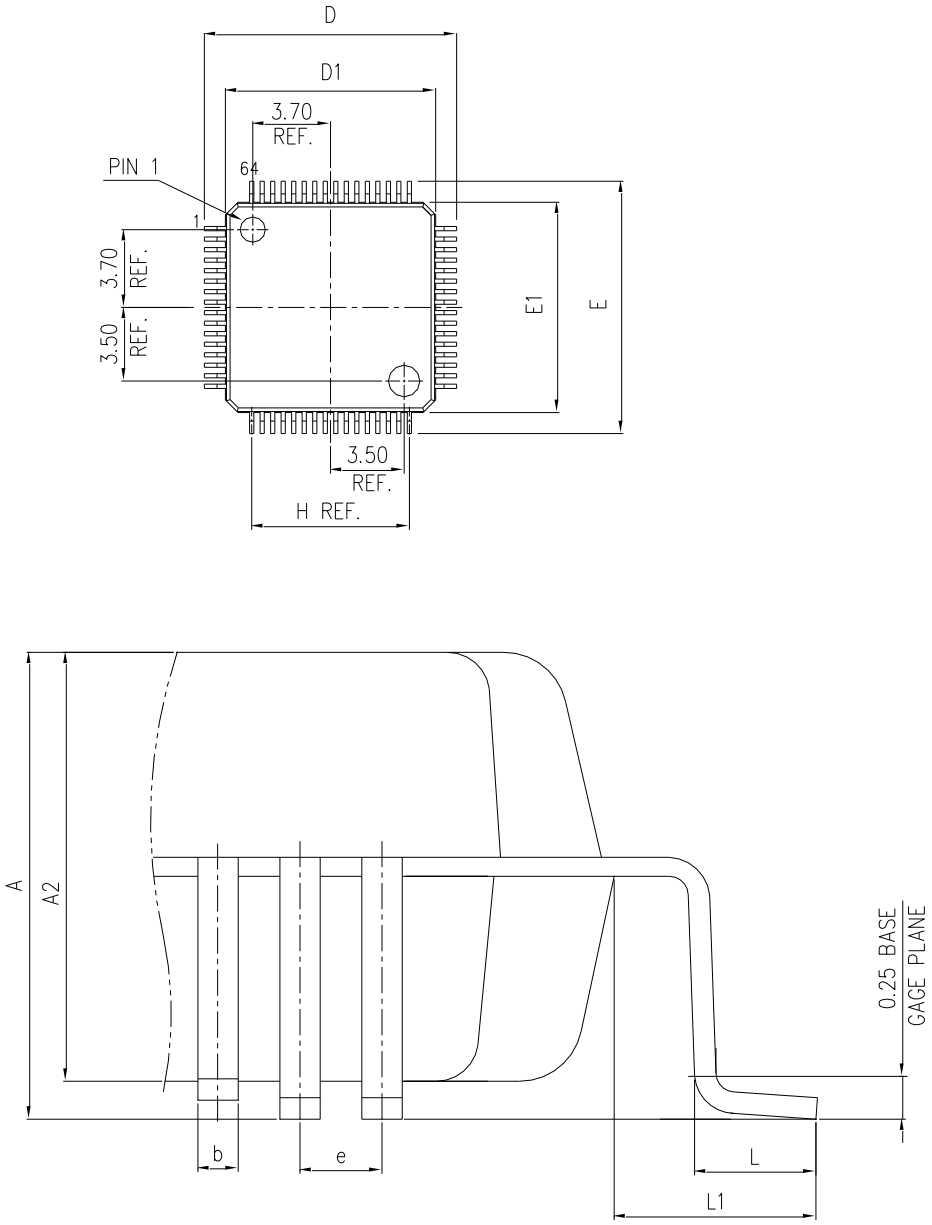
Note: Dimensions are marked in millimeters.

Figure 9 LQFP100 - 100 Pins, 14 x 14mm Diagram



7.2 LQFP64 package information

Figure 10 LQFP64 Package Diagram



(1) The figure is not drawn to scale.

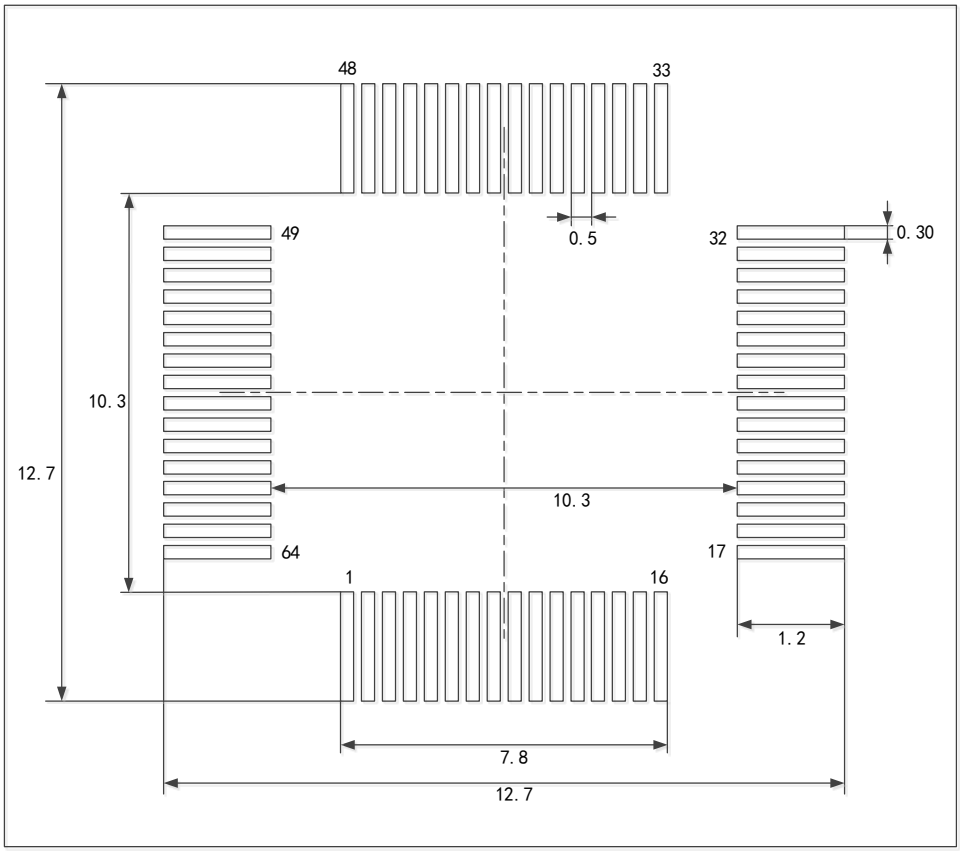
(2) All pins should be soldered to the PCB.

Table 15 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALLHEIGHT
2	A2	1.400±0.050	PKGTHICKNESS
3	D	12.000±0.200	LEADTIPTOTIP
4	D1	10.000±0.100	PKGLENGTH
5	E	12.000±0.200	LEADTIPTOTIP
6	E1	10.000±0.100	PKGWIDTH
7	L	0.600±0.150	FOOTLENGTH
8	L1	1.000REF.	LEADLENGTH
9	e	0.500BASE	LEADPITCH
10	H(REF.)	(7.500)	GUM.LEADPITCH
11	b	0.220±0.050	LEADWIDTH

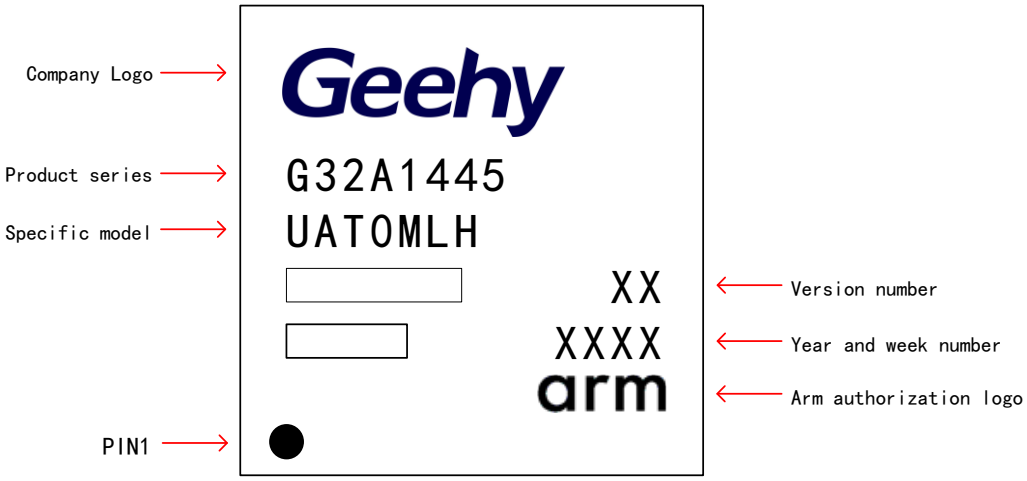
Note: Dimensions are marked in millimeters.

Figure 11 LQFP64 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

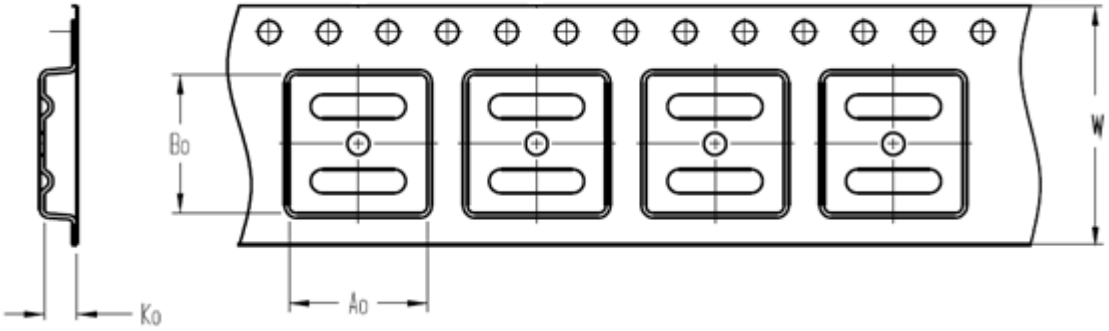
Figure 12 LQFP64 - 64 Pins, 10 x 10mm Diagram



8 Packaging Information

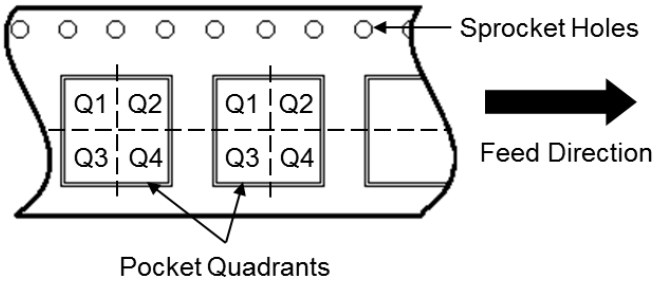
8.1 Reel Packaging

Figure 13 Reel Packaging Specification Drawing

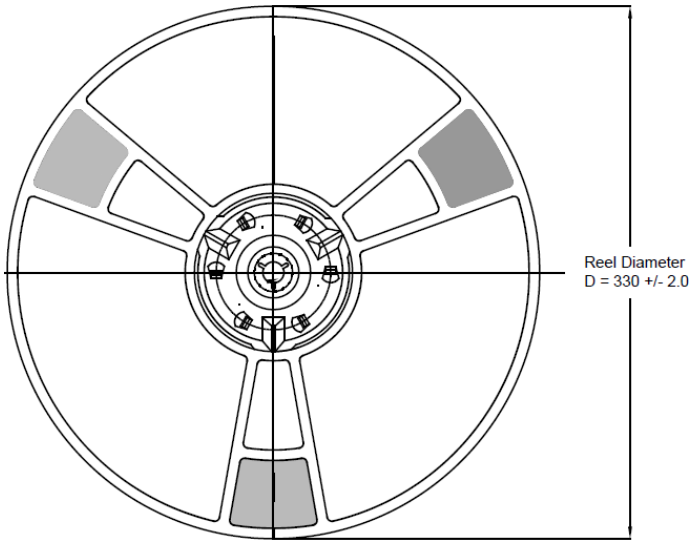


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions



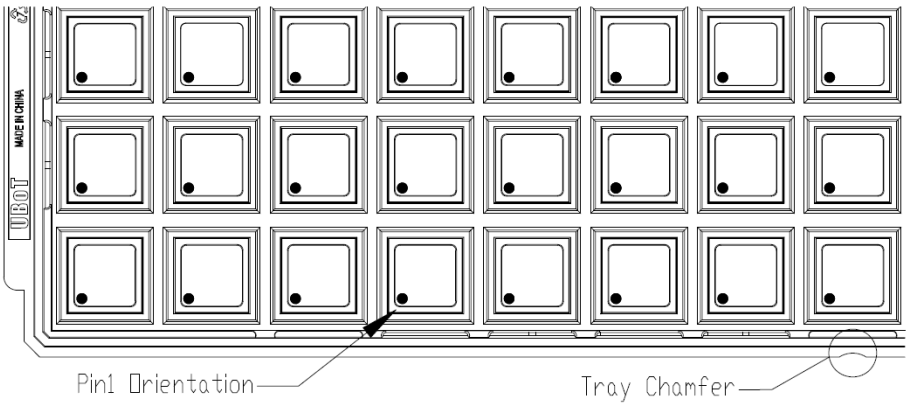
All photos are for reference only, and the appearance is subject to the product.

Table 16 Reel Packaging Parameter Specification Table

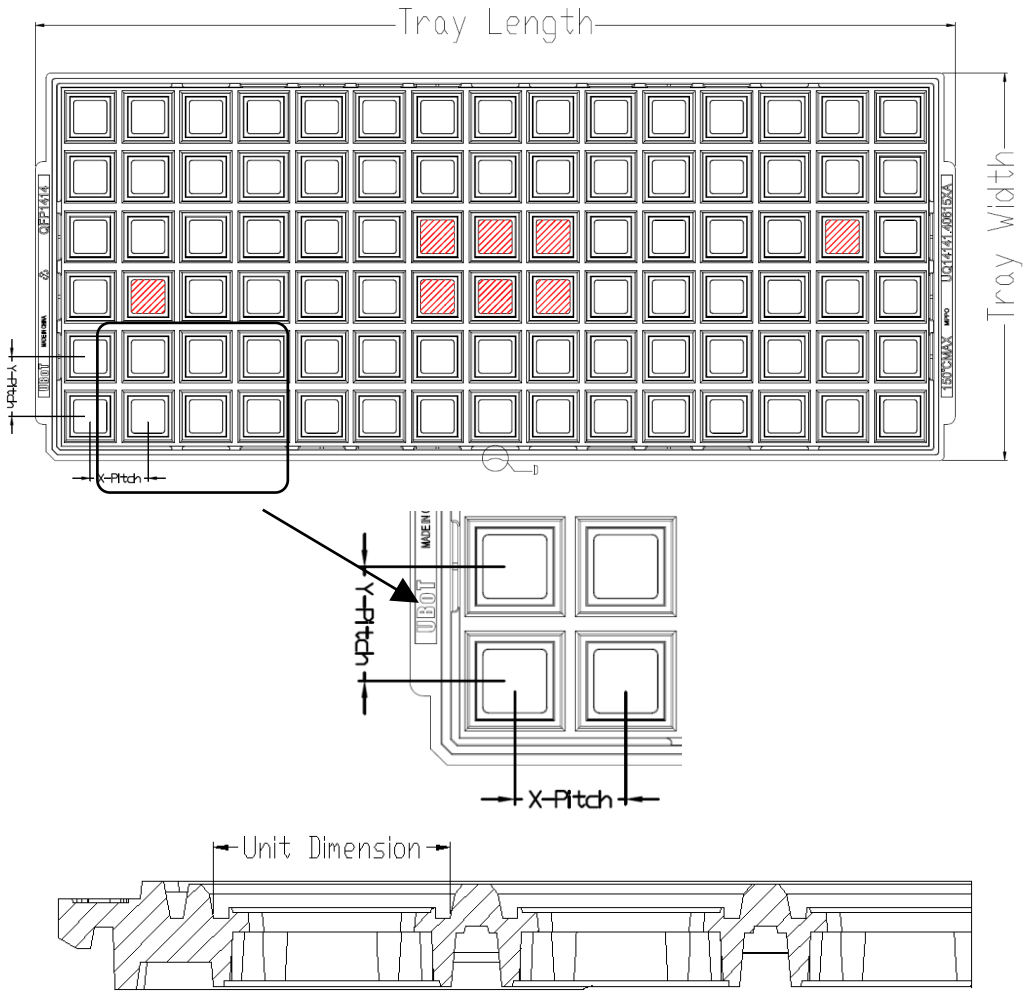
Device	Package Type	Pins	SPQ	Reel Diameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
G32A1445UAT0MLHR	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32A1445HAT0MLHR	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32A1445UAT0VLHR	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1
G32A1445HAT0VLHR	LQFP	64	1000	330	12.35	12.35	2.2	24	Q1

8.2 Tray packaging

Figure 14 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product

Table 17 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32A1445UAT0MLLT	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32A1445HAT0MLLT	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32A1445UAT0VLLT	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32A1445HAT0VLLT	LQFP	100	900	16.6	16.6	20.3	21	322.6	135.9
G32A1445UAT0MLHT	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32A1445HAT0MLHT	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32A1445UAT0VLHT	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32A1445HAT0VLHT	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9

9 Ordering Information

Figure 15 Product Information Naming Rules

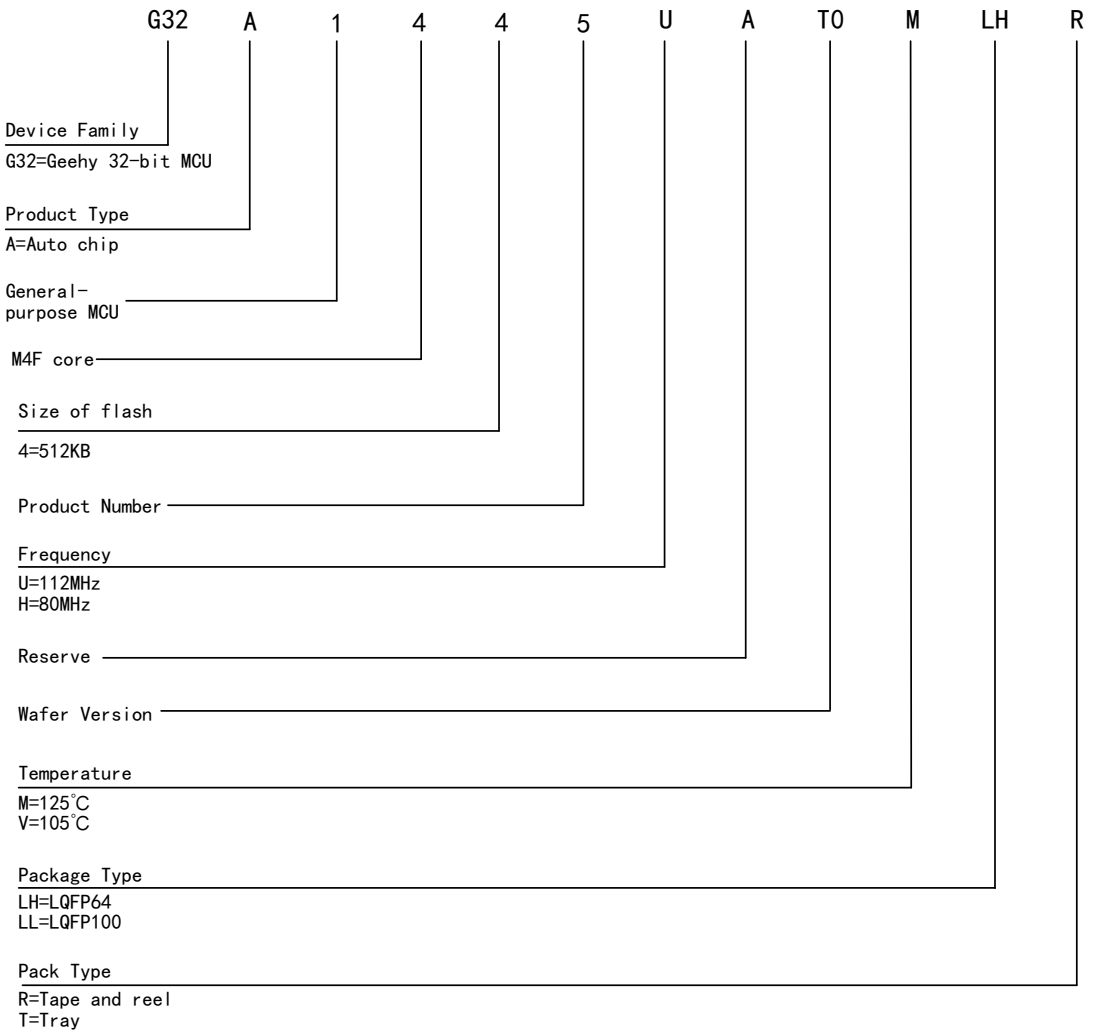


Table 18 Ordering Information Table

Order Code	Dominant frequency	Flash (KB)	SRAM (KB)	EEPROM (KB)	Package	SPQ	Temperature range
G32A1445UAT0MLHT	112MHz	512	64	4	LQFP64	1600	-40℃~125℃
G32A1445HAT0MLHT	80MHz	512	64	4	LQFP64	1600	-40℃~125℃
G32A1445UAT0MLHR	112MHz	512	64	4	LQFP64	1000	-40℃~125℃
G32A1445HAT0MLHR	80MHz	512	64	4	LQFP64	1000	-40℃~125℃
G32A1445UAT0VLHT	112MHz	512	64	4	LQFP64	1600	-40℃~105℃
G32A1445HAT0VLHT	80MHz	512	64	4	LQFP64	1600	-40℃~105℃
G32A1445UAT0VLHR	112MHz	512	64	4	LQFP64	1000	-40℃~105℃
G32A1445HAT0VLHR	80MHz	512	64	4	LQFP64	1000	-40℃~105℃

Order Code	Dominant frequency	Flash (KB)	SRAM (KB)	EEPROM (KB)	Package	SPQ	Temperature range
G32A1445UAT0MLLT	112MHz	512	64	4	LQFP100	900	-40℃~125℃
G32A1445HAT0MLLT	80MHz	512	64	4	LQFP100	900	-40℃~125℃
G32A1445UAT0VLLT	112MHz	512	64	4	LQFP100	900	-40℃~105℃
G32A1445HAT0VLLT	80MHz	512	64	4	LQFP100	900	-40℃~105℃

Note: SPQ: Smallest Packaging Quantity.

10 Commonly Used Function Module Denomination

Table 19 Commonly Used Function Module Denomination

Full name	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Window watchdog timer	WWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller local area network	CAN
I2C Interface	I2C
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC
Secure digital input/output	SDIO
Digital camera interface	DCI

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